4

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/054,241	01/22/2002	John K. Walton	EMC2-078AUS	4075

45456 7590 01/18/2005

RICHARD M. SHARKANSKY
PO BOX 557
MASHPEE, MA 02649

EXAMINER	
ELAMIN, ABDELMONIEM I	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 01/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/054,241	WALTON ET AL.	
	Examiner	Art Unit	
	A Elamin	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,19-26,28-35 and 38-59* is/are rejected.

7)☒ Claim(s) *17,18,27,36 and 37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/16/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims *11, 20-21, 29-30, 39-40, 44, and 48-55* are rejected under 35 U.S.C. 102(b) as being anticipated by Komachiya et al, Japanese Pat. No. JP 7-302171 (*cited by Applicant*).

3. Claims *11, 20-21, 29-30, 39-40, 44, and 48-55*, Komachiya teaches a data storage system wherein end-user data is transferred between a host computer and a bank of disk drives through an interface, such interface [*see Fig. 1*], comprising:

a memory [*cache memory 19 of Fig. 1*];

a plurality of directors [*CDCs 5 and DDCs 13 of Fig. 1*], at least one front-end one of the directors being in communication with the host computer [*CPU of Fig. 1*]and at least one rear-end one of the directors being in communication with the bank of disk drives [*drives 12 of fig. 1*], each one of the directors comprising:

a central processing unit [*inherently, directors comprise a CPU*];

an interface state data bus section [*the common bus CBS 8 of Fig. 1*], for carrying interface state data, such interface state data bus section being in communication with both:

(a) the at least one front-end one and the at least one rear-end one of the directors [*see Fig. 1*]; and

(b) the memory [*see Fig. 1*];

a plurality of end-user data busses [*Fig. 1, see also paragraph 2, page 19*], for carrying end-user data, each one of the plurality of end-user data busses having a first end coupled to a corresponding one of the plurality of directors and a second end coupled to the memory [*through DBS 7 of Fig. 1*]; and

wherein the central processing units of such plurality of directors control the end-user data transfer between the host computer and the bank of disk drives through the memory via the end-user data busses in response to interface state data generated by the directors, such generated interface state data being transferred among the directors via the interface state data bus section [*pages 19-20*].

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims *12-16, 19, 22-26, 28, 31-35, 38, 41-43 and 45-47* rejected under 35 U.S.C. 103(a) as being unpatentable over Komachiya et al, Japanese Pat. No. JP 7-302171.

6. Claims *12, 22, 31, 41-43 and 45-47*, Komachiya fails to teach the end user data buses are serial busses.

Official notice is taken that both the concept and the advantages of serial busses is old

and well known in the art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Komachiya to include serial busses, because it allows to reduce the costs of the system.

7. Claim, *13, 23, and 32,* Komachiya fails to teach the interface state data bus section includes parallel busses.

Official notice is taken that both the concept and the advantages of parallel busses is old and well known in the art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Komachiya to have the interface state data bus section includes parallel busses, because it provides a fast transfer rate.

8. Claim *14, 24 and 33*, Komachiya fails to teach coupling parallel busses to the directors in a multi-drop configuration.

Official notice is taken that both the concept and the advantages of multi-drop configuration is old and well known in the art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Komachiya to include coupling parallel busses to the directors in a multi-drop configuration, because it allows new components to be easily added or even be ported between components that use a common multi-drop bus.

9. Claims *15, 25 and 34*, Komachiya fails to teach the end user data buses are serial buses.

Official notice is taken that both the concept and the advantages of serial busses is old and well known in the art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Komachiya to include serial busses, because it allows to reduce the costs of the system.

10. As to claim *16, 19, 26, 28, 35 and 38,* Komachiya fails to teach the parallel busses are coupled to the directors in a multi-drop configuration.

Official notice is taken that both the concept and the advantages of multi-drop configuration is old and well known in the art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Komachiya to include coupling parallel busses to the directors in a multi-drop configuration, because it allows new components to be easily added or even be ported between components that use a common multi-drop bus.

11. Claims *56-59 are* rejected under 35 U.S.C. 103(a) as being unpatentable over Komachiya et al, Japanese Pat. No. JP 7-302171 in view of Murata, US. Pat. No. 5,386,511 (*cited by Applicant*).

12. Claims *56-59*, Komachiya fails to teach one of an end user data port and an interface state data port being coupled to a crossbar switch.

Murata teaches a multiprocessor system comprising a plurality of processors [*processors 1a-1n of Fig. 2*]; a main memory comprising a plurality of memory modules [*memory modules 9a-9n of Fig. 2*]; an interconnection network for selectively connecting the plurality of the processors to the memory modules [*abstract, Fig. 2*].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Komachiya and Murata, because this would increase the system bandwidth [*see Murata, abstract*].

Allowable Subject Matter

13. Claims *17-18, 27 and 36-37* are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A Elamin whose telephone number is (571) 272-3674. The examiner can normally be reached on MON-FRI 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A Elamin
Primary Examiner
Art Unit 2116

January 12, 2005